SESAME Synchrotron-light for Experimental Science And Applications in the Middle East	**Technical Sector**
	Subject : RF — More specified area: Digital Low Level RF
	Date: 6/23/2010 — Total Number of Pages: *11*
	Document type: *Technical notes*
	Document No. : **SES-TS-GE-RF – 10/1-v-1**

Title :

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Distribution List: Technical director and technical staff
Access: Both internet and Intranet

Revision table

Rev #	*date*	*Done by*	*Remarks*
1	*6/23/2010*	*Tasaddaq A. Khan, Arash Kaftoosian, Darweesh Foudeh*	*This report is the first technical note on SESAME Digital Low Level RF*
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Digital Low Level RF for SESAME

Tasaddaq Ali Khan, Arash Kaftoosian, Darweesh Foudeh

Abstract

Low Level Radio Frequency (LLRF) is an essential part of RF systems of synchrotron light sources. It is used to regulate the amplitude, phase, and resonant frequency of the RF cavities by using control loops. The requirement of highly stable and precise RF fields and better RF diagnostics leads to develop Digital Low Level Radio Frequency (DLLRF) for the synchrotron facilities. State of the art in digital technologies makes it possible to develop DLLRF for achieving required degree of stability of RF parameters. This paper will present the study of the DLLRF as well as the proposed strategy for developing the DLLRF for SESAME.

Introduction

Basic function of low level electronics for radio frequency system (LLRF) is to regulate amplitude and phase of the accelerating voltage or field inside cavity, and also to tune the RF cavity. LLRF collects the data of amplitude and phase of cavity voltage and then processes the data by applying signal processing algorithms and the processed data is used to monitor, control, and regulate RF system parameters in the accelerators. LLRF could also be used to operate at different operating modes like conditioning, power-up sequencing, and normal operation.

The requirements for the RF control system have changed from only controlling the amplitude and phase of the accelerating field to the required degree of stability and operation close to performance limit. This is the reason to shift from analog LLRF to develop Digital LLRF (DLLRF). In this DLLRF control system, the RF signal is down-converted to the Intermediate Frequency (IF) signal while keeping the information in the signal preserved. This IF signal is sampled using analog to digital converter (ADC) at a constant sampling rate. Then a soft demodulator is used to obtain I and Q's components. Then controlled I and Q's are obtained by applying proper control algorithms on the demodulated I & Q's. A software limit switch is used to limit the output to reach too high values. Then DAC is applied to get back the analog I & Q and a modulator is used to get the regulated RF for the cavity.

In this DLLRF control system, there are three major components in cavity field control: Demodulation, processing the data, and modulation.

Down-Conversion

For the complete DLLRF system, the RF signal from a cavity must first be demodulated and converted to digital form. Due to the limitations of ADCs, digitization of high-frequency carrier signals is very often not possible or reasonable. This results in converting the RF signal to IF signal and the process is called heterodyning. This down conversion is done by the Mixers. An ideal mixer consists of two input ports and one output port. The signal at the output port is the vector multiplication of the signals at the two input ports.
If the signals are:

$$\begin{aligned} f_{RF}: &\quad y_{RF}(t) = A_{RF}\,.\sin(\omega_{RF}\,t + \varphi_{RF}) \\ f_{LO}: &\quad y_{LO}(t) = A_{LO}\,.\cos(\omega_{LO}\,t + \varphi_{LO}) \\ f_{IF}: &\quad y_{IF}(t) = y_{RF}(t).y_{LO}(t) \end{aligned}$$

Then

$$y_{IF}(t) = [A_{RF}\,.\sin(\omega_{RF}\,t + \varphi_{RF})].[A_{LO}\,.\cos(\omega_{LO}\,t + \varphi_{LO})]$$

$$y_{IF}(t) = \frac{1}{2}A_{RF}A_{LO}[\sin\{(\omega_{RF} - \omega_{LO})t + (\varphi_{RF} - \varphi_{LO})\} + \sin\{(\omega_{RF} + \omega_{LO})t + (\varphi_{RF} + \varphi_{LO})\}]$$

where

$\sin\{(\omega_{RF} - \omega_{LO})t + (\varphi_{RF} - \varphi_{LO})\}$ is the lower side-band

and

$\sin\{(\omega_{RF} + \omega_{LO})t + (\varphi_{RF} + \varphi_{LO})\}$ is the upper side-band

As upper side-band is not required in this case, so by applying low pass filter the lower side-band can be obtained, and the above equation will become

$$y_{IF}(t) = \frac{1}{2}A_{RF}A_{LO}[\sin\{(\omega_{RF} - w_{LO})t + (\varphi_{RF} - \varphi_{LO})\}]$$

$$\Rightarrow \quad y_{IF}(t) = A_{IF}\,.\sin(\omega_{IF}\,t + \varphi_{IF})$$

where

$$\omega_{IF} = (\omega_{RF} - \omega_{LO})$$

$$A_{IF} = \frac{1}{2}A_{RF}\;A_{LO} \sim A_{RF} \qquad with\ constant\ A_{LO}$$

$$\varphi_{IF} = \varphi_{RF} - \varphi_{LO} \sim \varphi_{RF} \qquad with\ constant\ \varphi_{LO}$$

This shows that keeping the LO signal constant (means keeping amplitude and phase constant), the amplitude and phase of the down converted signal is directly proportional

to the input signal, in other words, all the basic properties of an RF signal are conserved in the frequency conversion process.
Ideal mixers are linear while real mixers are non-linear in nature. The output spectrum of the real mixers is not two signals (upper and lower band) but the output contains undesired signals at $mf_{RF} \pm nf_{LO}$. So, after the mixer adequate low pass filters are applied in order to get the desired low band signal.

IQ Sampling

In circular accelerators, digital IQ sampling is common technique to control amplitude and phase of the RF signals. In digital IQ sampling, the RF signal is first converted to IF signal and then directly digitized so the information in I/Q is extracted in a digital way.

The sinusoidal RF signal

$$\mathrm{y(t)} = A.\sin(\omega t + \varphi_0)$$

can be modeled as a phase which is rotating vector with amplitude A, frequency w, and an initial phase φ_0.

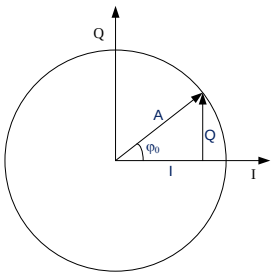

Figure 1: Phasor diagram to show amplitude and phase

The above equation can be written as:

$$y(t) = A.cos\varphi_0\ \sin(\omega t) + A.sin\varphi_0 \cos(\omega t) \qquad (1)$$
$$y(t) = \ \ I.\ \ \mathrm{Sin}(\omega t) \qquad + \quad Q\ .cos(\omega t) \qquad (2)$$

where

$$I = A.cos\varphi_0 \quad \& \quad Q = A.sin\varphi_0$$

From above equations, the amplitude A and phase φ_0 can be calculated as:

$$A = \sqrt{I^2 + Q^2}$$
$$\varphi_0 = \tan^{-1}\left(\frac{Q}{I}\right)$$

The equation (2) shows that amplitude of sine component can be defined as in-phase component (I), while the amplitude of the cosine component is called the quadrature-phase component (Q).

Usually IQ sampling is achieved if the sampling frequency f_s and IF frequency f_{IF} are related by:

$$f_s = 4.f_{IF}$$

In this case the phase difference between two consecutive samples will be 90^0, so from equation (2),

$$\begin{aligned} \omega t_0 &= 0, & y(t_0) &= Q \\ \omega t_1 &= \frac{\pi}{2}, & y(t_1) &= I \\ \omega t_2 &= \pi, & y(t_2) &= -Q \\ \omega t_3 &= \frac{3\pi}{2}, & y(t_3) &= -I \end{aligned}$$

This gives a sequence of $Q, I, -Q, -I,$ ….. by using the phase shift of 90^0 the sequence $I, Q, -I, -Q,$…. will be obtained. Then by applying the sign swap or software switch the sequence I, Q, I, Q…. can be obtained.
The idea of choosing a sampling frequency four times of the carrier frequency is to simplify the calculation as the rotation matrix will just consist of 1, 0, -1. Generally, the sampling frequency is chosen as following

$$\frac{f_s}{f_{IF}} = m \qquad where\ m\ is\ an\ integer$$

And in this case, the phase difference between two samples will be:

$$\Delta\varphi = \frac{2\pi}{m}$$

IQ demodulation is mainly used in feedback applications where very short latency is important and where the sampling frequency can be locked to the IF.

As the mixers are non-linear devices and ADCs produce differential non-linearities, so these two devices generate higher harmonics of the input signal frequency f_{IF}. Since in

IQ sampling the signal is sampled four times in a cycle so second harmonics maps on the Nyquist frequency while third harmonics map to IF frequency. In general, all odd harmonics lie on the IF frequency and even harmonics map on DC or Nyquist frequency. Standard IQ sampling technique can't distinguish the harmonics that maps on the IF frequency.

This problem can be solved by using non IQ sampling technique. For non-IQ sampling case, following relation holds:

$$f_s = \frac{N}{M} \cdot f_{IF}$$
$$\Rightarrow \quad M.f_s = N.f_{IF}$$

The phase difference between two consecutive ADC readings in case of non-IQ sampling is

$$\Delta\varphi = 2\pi.\left(\frac{M}{N}\right)$$

as compared to 90^0 in case of IQ sampling. But the latency in case of IQ sampling is lower as compared to non-IQ sampling so cost will also be low in case of IQ sampling.

Up-Conversion or Modulation

In order to control the RF signal, it is necessary to convert baseband signal to a real pass-band signal. This process could be done with mixers or simply modulators. Basically, there are two types of up-conversion techniques:

Homodyne Up-conversion:

In this scheme, a vector modulator is used to generate the required RF by mixing the analog baseband I &Q signals to the in-phase and quadrature-phase components of the RF. In this case, there is no need of IF. The mixers in the vector modulator are operated as amplitude control elements.
Output RF signal can be written as:

$$RF_{out}\ (t) = A_{out} \cdot \sin(\omega t + \varphi_0)$$

where

$$A_{out} = A_{RF}.\sqrt{I^2 + Q^2}$$
$$\varphi_0 = \tan^{-1}\left(\frac{Q}{I}\right)$$

With this approach, pure amplitude or a pure phase modulation can be implemented very easily. In case of homodyne up-conversion, the DAC selected should be of DC output coupling.

Heterodyne Up-conversion:

In this case, I & Q signals are digitally converted to analog IF signal by DAC. This process is known as Heterodyne up-conversion or IF up-conversion. This analog IF signal is again mixed with LO to get the required RF. In the mixing process unwanted image frequency is also obtained that can be removed by using high pass filter. This mixing process is called double-sideband modulation as both the desired RF as well as the image frequency is generated. Since, in this technique the conversion of I & Q to IF signal is done digitally so it is not susceptible to gain imbalance and quadrature skews. But the DACs must provide higher bandwidth that will result in errors like pass-band ripples and harmonics distortion.

Controller

Proportional Integration (PI) controller is mostly used in DLLRF to control the values of I and Q. PI controller is the combination of proportional (P) and integral (I) controller. Proportional controller means that the system responds in proportion to how far it is from the set point, basically proportional controller reduces the rise time, increases the overshoot, and reduces the steady state error but it never eliminates the steady state error. While on the other hand, integral controller means that the system will respond in proportion to the integral of the error over time. An integral controller decrease the rise time, increases both the overshoot and settling time, and eliminates the steady-state error but it may make the transient response worse. So, proportional controller allows us to quickly move to the set point when we are far away and integral controller allows us to accurately stay around the set point – compensating for the proportional offset problem. By using PI controller, one will almost certainly reach to its target by properly using gain values. Tuning is simple but time consuming process. First, set both P and I gains to zero, then increase K_P (proportional gain) until response reaches where you like it and there you will get steady-state error. Then start increasing K_I (integral gain) slowly, the goal is to drive it smoothly to the target point.
Basic scheme of PI controller is shown in figure 2:

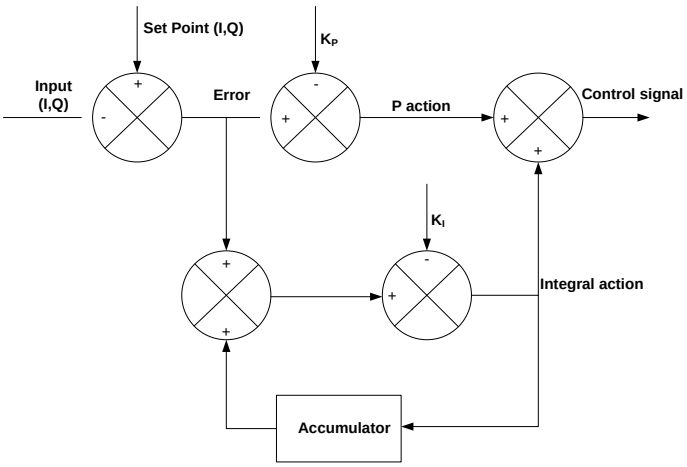

Figure 2: PI Controller block diagram

SESAME DLLRF

The main objective of the SESAME DLLRF will be to control the amplitude (within the accuracy of 1%), phase (within ±0.5^{o}), and to tune RF cavity (100kHz or more). It will consist of two basic feedback loops:

1. First loop is called field control loop and will be used to regulate the amplitude and phase of the RF field
2. Second loop that is called the tuning loop will be used to compensate for the transient beam loading and cavity temperature variation

Hardware

The development of state of the art digital hardware such as digital signal processing (DSP) and Field Programmable Gate Arrays (FPGAs) as well as software tools like VHDL and Verilog allows real time digital control systems to be implemented with relative ease. Large gate density and other hardware features of FPGA helps in implementing state of the art and complex algorithms to process the data in real time. I/Q control loops and CORDIC algorithms can be implemented in FPGA to regulate the amplitude, phase, and tuning of the cavity respectively.

At SESAME, COTS (commercial of the shelf) hardware will be used to implement the software for the control loops. High resolution ADCs and DACs will be used to get good accuracy that was not possible some years ago. Analog front ends for the up-conversion and down-conversions alongwith timing modules to provide Local Oscillator (LO) signal

and digital clocks will be developed locally. IF signal will be obtained by applying mixers and appropriate low pass filters. Care must be taken while choosing mixer and LO regarding the phase noise. For modulation or analog front end for the up-conversion, a better solution is to use homodyne up-conversion technique. So, DACs with DC coupling will be chosen in order to get controlled DC output to modulate the RF signal.

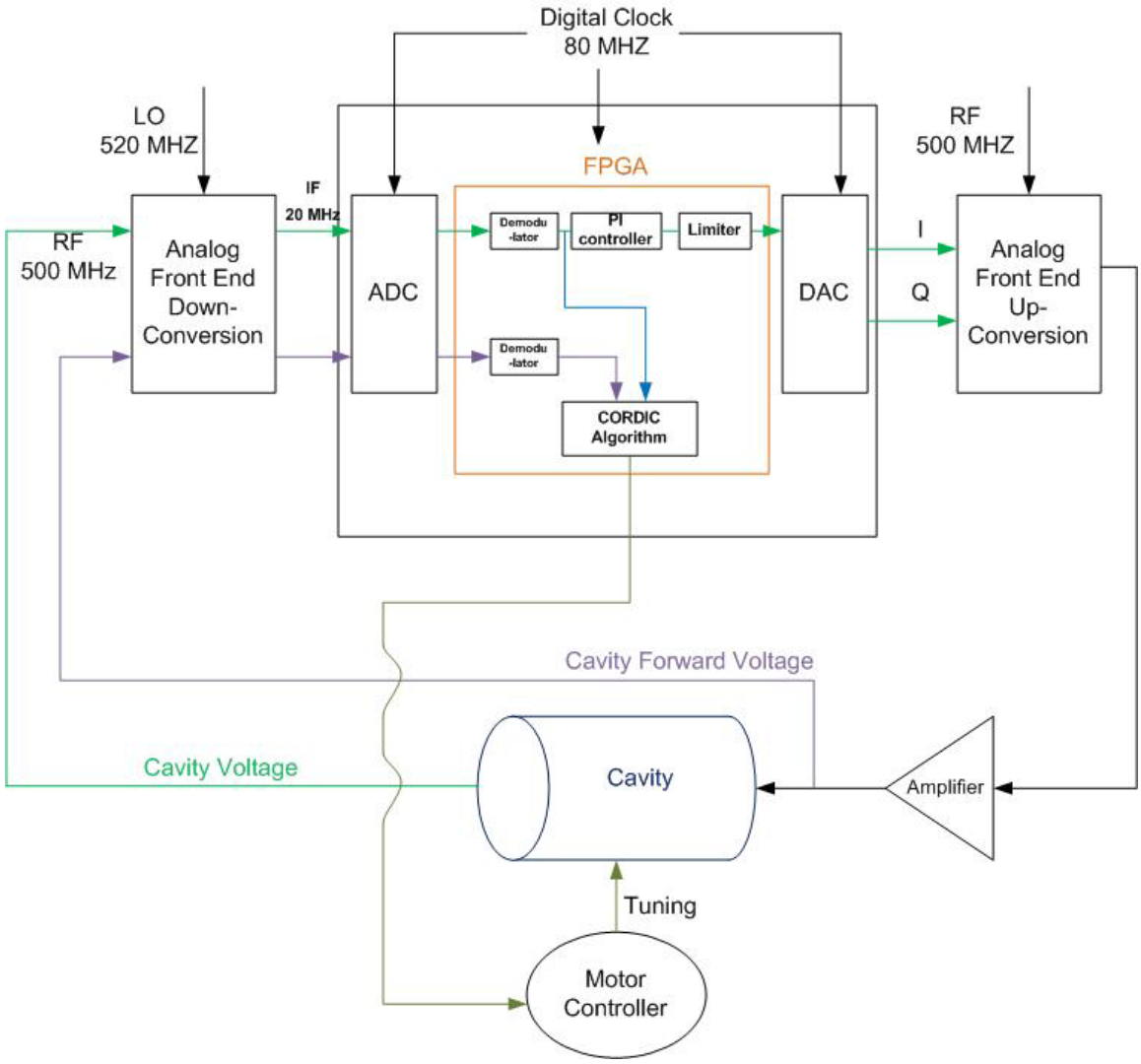

Figure 3: Proposed SESAME DLLRF system architecture

Timing system is one of the most important hardware in DLLRF. Timing system will generate LO signal for down-conversion and also it will generate digital clocks. The Local Oscillator will be used to produce IF signal while the digital clock will be provided to

ADCs, DACs, and FPGA. To develop a good timing system, the sampling clock (digital clock) and LO must be phase locked to the reference frequency (500 MHz). When the sampling clock is not phase-locked to the signal frequency, I/Q demodulation schemes can't generate phase information without a large amount of calculation.

Software

Matlab/Simulink is a powerful tool to simulate non-linear dynamic systems. It will be used to develop the DLLRF model to simulate the system response and also to optimize different control parameters by performing stability analysis. Then this model will be implemented in VHDL. The software scheme will work as follows:
IQ sampling technique will be used over non-IQ sampling technique due to its advantage of easy implementation. A soft demultiplexer will be used to separate I and Qs in the data stream and the sequence of the data stream will look like I, Q, -I, -Q, I, Q …. By applying sign swapping method the data will become I, Q, I, Q …. Amplitude and phase of RF in the cavity can be controlled by controlling I/Q. So, PI controller with appropriate set values will be used to control I & Q. Proportional and integral gains will be adjusted by monitoring response of PI controller at different gain values. Lastly, a limiter will be introduced to limit the value of I and Q for reaching too high values.
For tuning of the cavity, CORDIC algorithm will be implemented to calculate the phase difference between the cavity voltage and cavity forward power.

Conclusion

In the first phase, proper IF will be selected, the analog front ends will be developed, and also selection of proper card will be done. In the meantime a software model will be developed using Matlab/Simulink. In the second phase, all the loops will be implemented in the hardware using VHDL and verify the design. Finally, it will be connected to the cavities for real time simulation.

Acknowledgement

The authors would like to thank Angela Salom and Dr. Francis Perez of ALBA RF group for providing help for understanding the DLLRF. Special thanks to Dr. Dieter Einfield for providing the opportunity to visit ALBA to see the state of the art in RF group.

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